REMARKS/ARGUMENTS

The office action of December 31, 2002 has been carefully reviewed and these remarks are responsive thereto. Reconsideration and allowance of the instant application are respectfully requested. Claims 1-15 remain pending in this application. Claims 1, 6 and 11 have been amended. Claims 16 and 17 have been added.

Preliminarily, Applicants note with appreciation, the Examiner's indication that the application contains allowable subject matter. Specifically, claim 11 would be allowable if amended to overcome a rejection under 35 U.S.C. § 112, second paragraph. Since claims 12-15 depend from claim 11 and were rejected for the same reasons as claim 11, it would appear that they also would be allowable if claim 11 is amended to overcome the rejection under 35 U.S.C. § 112, second paragraph.

Applicants are filing an Information Disclosure Statement including a copy of U.S. patent no. 6,449,727 ('727 patent). In an Information Disclosure Statement in the parent of the instant application, applicants identified the related application (by serial no.), which matured into the '727 patent. Since then, the application has issued and for completeness, applicants are now submitting a copy of the issued patent.

Applicants note that U.S. Patent No. 5,708,382 to Park applied by the Examiner to reject certain claims of the instant application has not been made of record on a PTO Form 892. Thus, applicants respectfully request the Examiner to return a PTO Form 892 with the next communication formally making the Park patent of record.

Claims 1-15 stand rejected under 35 U.S.C. § 112, second paragraph, for indefiniteness. Applicants have amended independent claims 1, 6 and 11 to address the issues raised by the Examiner. It is believed that amended claims 1-15 are sufficiently definite to meet the requirements under 35 U.S.C. § 112, second paragraph. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 1 and 2 have been rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,708,382 to Park. Claim 3 stands rejected under 35 U.S.C. § 103(a) as being obvious over Park. Claims 4-10 stand rejected under 35 U.S.C. § 103(a) as being obvious over Park in

view of U.S. Patent No. 5,606,270 to D'Souza et al. ("D'Souza"). Applicants respectfully traverse these rejections.

The action alleges that Park shows all the features of claim 1. The action relies on inverter 31 and NOR gate 32 in Fig. 1 of Park to show the clocked inverter circuit and logic circuit recited in claim 1. In stark contrast to Park, the amended claim 1 invention calls for, among other features, a clocked inverter circuit to which a first pulse signal is supplied, the clocked inverter circuit outputting a second pulse signal having one of a first pulse width and a second pulse width, the first pulse width being greater than a pulse width of the first pulse signal and the second pulse width being smaller than the pulse width of the first pulse signal; and a logic circuit to which the second pulse signal output from the clocked inverter circuit and an inverted signal of the first pulse signal are supplied, wherein the logic circuit outputs a third pulse signal to which the second pulse signal output from the clocked inverter circuit and an inverted signal of the first pulse signal are supplied, the third pulse signal having the other one of the first pulse width and the second pulse width. Notably, the circuits C1-C5 of Park, which include inverter 31 and NOR gate 32, are comparing circuits, and they do not act as a delay circuit as claimed. Namely, the NOR gate 32 does not teach or suggest a logic circuit to which the second pulse signal output from the clocked inverter circuit and an inverted signal of the first pulse signal are supplied, the third pulse signal having the other one of the first pulse width and the second pulse width. Rather, the NOR gate 32 (comparing circuit C1) of Park receives the inverted signal of Q1 from the inverter 31 and a signal Q2 output from the flip flop FF2. The signal Q2 of Park is not the inverted signal of the first pulse signal. Nor is the signal Q2 output from the inverter 31. Even more telling is that Consequently, neither the NOR gate 32 nor any other portion of Park teaches or suggests a logic circuit as called for in claim 1. For at least this reason, claim 1 is patentably distinct from Park. Claims 2 and 3, which depend from claim 1, are patentably distinguishable from Park for at least the same reasons as claim 1, and further in view of the novel features recited therein.

The action combines D'Souza with Park to show the features of claims 4 and 5, which depend from claim 1. Notwithstanding the propriety of the combination, D'Souza fails to remedy the deficiencies noted above with respect to Park. Namely, D'Souza provides no teaching or

suggestion of the logic circuit of claim 1. Thus, the combination of Park and D'Souza, even if proper, does not result in the invention of claims 1, 4 and 5.

As amended, independent claim 6 calls for, among other features, an inverter circuit controlled by a clock signal to which a first pulse signal is supplied, the inverter circuit outputting a second pulse signal having one of a first pulse width and a second pulse width, the first pulse width being greater than a pulse width of the first pulse signal and the second pulse width being smaller than the pulse width of the first pulse signal; and a logic circuit to which the second pulse signal output from the inverter circuit and the inverted signal of said first pulse signal are supplied, wherein the logic circuit outputs a third pulse signal, the third pulse signal having the other one of the first pulse width and the second pulse width.

To show the claim 6 combination of features, the action relies on the combination of Park and D'Souza. However, neither Park alone nor in combination with D 'Souza, even if proper, teaches or suggests the logic circuit of claim 6. Indeed, NOR gate 32 of Park receives the inverted signal of Q1 from the inverter 31 and a signal Q2 output from the flip flop FF2. The signal Q2 of Park is not the inverted signal of the first pulse signal. Nor is the signal Q2 output from the inverter 31. D'Souza fails to remedy these defects. Hence, for at least these reasons, claim 6, and claims 7-10, which ultimately depend from claim 6, are patentably distinct from the combination of Park and D'Souza.

New claims 16 and 17 are fully supported by the specification and considered patentably distinct over the art of record. For example, none of the prior art of record teaches or suggests a delay circuit as recited in claim 16 including a clocked inverter circuit to which a first pulse signal is supplied, the clocked inverter circuit outputting a second pulse signal having a pulse width wider than a pulse width of the first pulse signal; and a logic circuit to which the second pulse signal output from the clocked inverter circuit and an inverted signal of the first pulse signal are supplied, wherein the logic circuit outputs a third pulse signal, the third pulse signal having a pulse width narrower than the pulse width of the second pulse signal and equal to the pulse width of the first pulse signal.

CONCLUSION

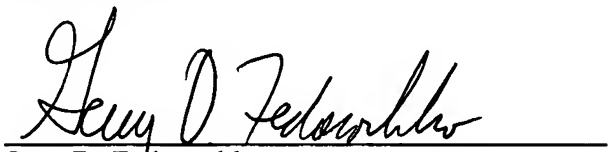
If any fees are required or if an overpayment is made, the Commissioner is authorized to debit or credit our Deposit Account No. 19-0733, accordingly.

All rejections having been addressed, applicants respectfully submit that the instant application is in condition for allowance, and respectfully solicit prompt notification of the same.

Respectfully submitted,

BANNER & WITCOFF, LTD.

Dated: March 26, 2003

By: 

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